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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,904	10/10/2000	Hironobu Kon	198092US-2S DIV	2551

22850 7590 09/19/2002

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EXAMINER
FARAHANI, DANA

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,904	KON ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *19 July 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa et al. (U.S. 5,874,750), previously cited.

Referring to figures 3, 4 and 5, Yanagisawa et al. disclose an injection enhanced gate transistor made of a semiconductor chip, comprising: a collector electrode formed on the back of the chip 10 (column 4, lines 43-44); a gate 13 formed on an opposing side, which opposes the one side of the semiconductor chip (Fig.4); a main emitter 12 formed on the opposing side of the semiconductor chip and a current sense emitter 12a formed on the opposing side of the semiconductor chip same side with the main emitter, figure 4; wherein electrical current form the collector is made to flow to both the main emitter and the current sense emitter (Fig.3).

Yanagisawa et al. discloses the claimed invention except for the electron injection efficiency at the main emitter and the current sense emitter being 0.73. It would have been obvious to one having ordinary skill in the art at the time the invention was made to keep electron injection efficiency at the main emitter and the current sense emitter being 0.73, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 24-32 are rejected under 35 U.S.C. 103(x) as being unpatentable over Yanagisawa et al. in view of Takeda et al. (1200 V Trench gate NPT-IGBT (IEGT) with Excellent Low On-State Voltage, Proceedings of 1998 International Symposium on Power Semiconductor Devices &Ics, Kyoto, pages 75-79), previously cited.

Yanagisawa et al. discloses the instant invention including: a plate-like collector electrode terminal 18 arranged on the one side of the power semiconductor device and electrically connected to the collector (Fig.4 and column 4, lines 64-65); a plate-like emitter electrode terminal 16 arranged on the one side of the power semiconductor device and electrically connected to the emitter (Fig.4, column 4, lines 64-65); wherein the voltage- driven power semiconductor device is a press-contacting type package (abstract, lines 1-2).

Yanagisawa et al. disclose the instant invention except for the gate of the injection enhanced gate transistor being a trench-type gate embedded in the opposing side of the chip, carrier accumulation efficiency of the main emitter and the current sense emitter in On state being greater than that of an insulated gate bipolar transistor (IGBT). However, figure 1 of Takeda et al. shows the gate of the injection enhanced gate transistor being a trench-type gate embedded in the opposing side of the chip, and figures 4 and 5 show carrier accumulation efficiency of the main emitter and the current sense emitter in On-state being greater than that of an insulated gate bipolar transistor in order to offer both sufficient margin for blocking voltage and low on-state voltage Device Design Section, page 75, right column, lines 2-3 form the bottom). It would have been obvious to one having ordinary skill in the art of the time the invention was made

to from the gate of the injection enhanced gate transistor being a trench-type gate embedded in the opposing side of the chip and the carrier accumulation efficiency of the main emitter and the current sense emitter in On-state being greater than that of an insulated gate bipolar transistor as taught by Takeda et al. in the device of Yanagisawa et al. to offer both sufficient margin for blocking voltage and low on-state voltage.

Response to Arguments

3. Applicant's arguments filed 7/19/02 have been fully considered but they are not persuasive.

Regarding applicant's argument that claims 23-32 require a "current sense terminal" which detects a current that flows into the main emitter so that an overcurrent, when detected, can be prevented. Applicant further argues that "this is an important property and advantage of the present invention" and Yanagisawa reference shows a voltage sense emitter in figure 3. Applicant concludes, "Clearly, Yanagisawa does not disclose a current sense terminal which senses the current flowing into the emitter electrode and itself, it only teaches and suggests emitter voltage sensing.

Yanagisawa discloses in column 6, lines 59-67, "according to said pressure-contact type IGBT, when sensing (monitoring) voltage of the emitter electrode 12 of the IGBT in order to detect an overcurrent and the like of the IGBT in a system using the IGBT, it is possible to directly measure voltage of the emitter sensing electrode 12a via the emitter voltage sensing terminal ES without using the emitter compression contact plate...". Voltage and current are linearly related by Ohm's law, and actually are

measured simultaneously with a gadget that measures and shows both the current and the voltage of any electrode, when needed, in an electronics laboratory. Therefore, applicant's allegation that Yanagisawa only teaches and suggests emitter voltage sensing is not true.

Regarding applicant's argument that "the outstanding Action errs in considers[ing] the limitation of the electron injection efficiency being 0.73 as being an optimum value of a result effective variable, the discovery of which involves only routine skill. However the conventional IGBT structure adopted by Yanagisawa would have a problem if the electron injection efficiency is provided as 0.73 or more because the injection efficiency would be too high at the emitter" applicant argues that this prevent the base voltage from controlling the switching operation between the collector and emitter. This is not found persuasive, since all NPN bipolar transistors (including the one in Yanagisawa reference) have electron injection efficiency (as defined in applicant's specification as electron current / total current) of 0.73 or more.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
September 15, 2002

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800